under 35 U.S.C. §112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Also, claims 10, 11, and 13-22 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicants regard as the invention. In light of the foregoing amendments and the discussion to follow, the objection and the rejections are respectfully traversed.

The remarks in the Amendment filed November 2, 1999, responding to the assertion that the original specification does not disclose interconnected transistors in and at the surface of the device silicon layer, as claimed in claims 1, 7, and 10, directed the Examiner's attention to FIG. 3g and its description at page 7, lines 5-7, of the instant specification: "FIG. 3g schematically shows in expanded cross-sectional elevation view a partially completed MOSFET in island 322, which would be just one of thousands of such devices in an integrated circuit fabricated on the bonded wafer." (Emphasis added) Clearly, the MOSFET depicted in FIG. 3g is located in and at the surface of device silicon layer 322, and, as one of many transistors included in an integrated circuit, would be connected with other transistors in the circuit. In paragraph 11 of the January 6 Office Action, the Examiner finds this argument unpersuasive on the grounds that the original specification never discloses these MOSFETs are connected with other transistors in the circuit. As stated in the original specification, the present invention relates to electronic integrated circuits and dielectrically isolated integrated circuits. By definition, the devices included in an integrated circuit are interconnected, i.e., connected with one another. Therefore the references to interconnected transistors at page 3, line 28, page 4, lines 4-5, and page 8, line 32 to page 9, line 2, in the specification and at page 16, lines7-8, 15-16, and 18 in the abstract are fully supported in the original disclosure and thus introduce no new matter.

In response to the objection to the sentence "The silicide layer...the silicide layer." at page 4, lines 9-11 of the specification, which is repeated in the abstract at page 26, lines 18-21 and also provides the basis for the more detailed description included in claim 10, the attention of the Examiner is respectfully directed to the description of FIGS. 5a-b on page 9, lines 5-21, which was present in the original specification. Handle die (512) comprises a first dielectric layer (oxide layer 513) that comprises a first bonding material (polysilicon 514) that bonds a silicide layer (WSi_2 515 formed from tungsten 518) to the first dielectric layer. Device wafer (502) includes a second dielectric layer (oxide layer 506) that comprises a second bonding material (polysilicon 517) that bonds the silicide layer to the second dielectric layer. A third

bonding material (aqueous solution of HNO_3 and H_2O_2 505) bonds the silicide layer to the handle die and the device wafer via the dielectric layers. Thus, it is clear that no new matter is introduced into the disclosure by the cited sentence in the specification and abstract.

As already noted, claims 4 and 5 are amended to depend on claim 7. In response to the assertion that the original specification never discloses a doped buried layer, as claimed in claim 4, or a diamond dielectric layer, as claimed in claim 5, the Examiner's attention is respectfully directed to page 7, lines 22-29, of the instant specification. Note in particular the specific reference to "diamond" at line 28.

On the basis of the foregoing discussion, withdrawal of the objection under 35 U.S.C. §132 and the final rejection of all the claims under 35 U.S.C. §112, first and/or second paragraphs, is respectfully requested.

Claims 1-4 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. Claim 5 has been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. and further in view of Sugimoto et al. Also claims 10, 11, 13, 14, 16, and 19-22 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. and further in view of Iwamatsu. Claims 15 and 17 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al. and further in view of Iwamatsu and Sugimoto et al. All these rejections are respectfully traversed.

There has been a persistent effort by the Examiner in the Office Actions relating to both the parent and the instant applications to show substantial similarity between the bonded structure of the present invention, one embodiment of which is depicted in Figures 4a-d, and the SOI wafer of Moslehi, represented in Figures 2a-f of the reference. Comparison of these figures and the supporting disclosures, however, reveals the gross dissimilarities between the applicants' structure and that of Moslehi.

As depicted in Figure 4b of the instant application, a continuous, unpatterned layer 415 of $CoSi_2$ overlies handle oxide layer 413. Figure 4c illustrates trenches extending through the silicide layer to form islands each with an underlying continuous silicide area. The Moslehi structure, on the other hand, includes, as shown in Figures 2e-f, a layer containing both a silicide (40) and a metal (e.g., titanium 24) in a grid pattern over oxide layer 22.

Further major differences exist between the integrated circuit of the present invention and the Moslehi structure. In the present invention, the silicide layer 415 lies between and is thereby adjacent to both first and second dielectric (oxide) layers 406 and 413, respectively, as shown in Figures 4b-d. The thin (500 angstroms thick, cf. page 7, lines 25-31) unpatterned polysilicon layers 417 and 414 shown in Figure 4(a) are substantially completely consumed in the reaction with Co to form silicide layer 415. In the Moslehi structure, by contrast, the grid-patterned layer containing silicide (40) and metal (24) is adjacent to a single oxide layer 22 and overlies a corresponding grid pattern of relatively thick (2 μm, cf. column 3, lines 22-23) polysilicon 38 and micro-vacuum chambers 42, a feature that is absent in the applicants' integrated circuit. The oxide layer 36 is spaced from the silicide layer 40 by the residual polysilicon 38.

The silicide layer 415 of the present invention constitutes a diffusion barrier to impurities. In the Office Action at page 7, third paragraph, the Examiner states that it is well known in the art that a metal silicide layer (emphasis added) can prevent diffusion of harmful ions into the device layer. However the metal-metal silicide grid structure of Moslehi, which exposes the copper wafer to contaminants, is clearly deficient as a diffusion barrier, as evidenced by the disclosure of and claims to an additional separate diffusion resistant layer of nitride adjacent to an oxide layer (cf. column 2, lines 28-30, claims 3-4). The continuous silicide layer of the present invention, by contrast, serves both as a bonding layer and as a diffusion barrier, no separate barrier layer being required.

See et al. is relied on for its teaching of bipolar and MOS transistors formed on a silicon substrate, and the Examiner states, at page 7, third paragraph, that the "combination of Moslehi and See et al. shows all the required elements of the claimed invention." Given the several major discrepancies between the teachings of Moslehi and the present invention, as emphasized in the preceding discussion, this assertion is clearly untenable. Similarly untenable is the Examiner's further assertion that the combination of the Moslehi and See et al. disclosures with that of Sugimoto et al., which is relied on solely for its disclosure of a diamond dielectric layer, "shows the required element of the dependent claim."

According to the Office Action, Iwamatsu shows that nitrogen can be implanted into a silicon dioxide layer. The disclosure of this reference is combined by the Examiner with the teachings of the three previously discussed references in finding claims 10, 11, and 13-22 unpatentable. Iwamatsu, in fact, teaches implantation at about three million electron volts of ions of Si, O, N, H, P, B, As, etc, into a silicon film, a procedure that has no relevance whatsoever to the present invention.

It is clear that the disclosures of See et al., Sugimoto et al., and Iwamatsu in no way remedy the gross deficiencies of the teachings of Moslehi with respect to the present invention. Withdrawal of the §103(a) final rejections of claims 1-5, 10, 11, and 13-22 as unpatentable over Moslehi and various combinations of See et al., Sugimoto et al., and Iwamatsu is respectfully requested.

Claims 7-9 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Ochiai, in view of Kameyama et al. Also, claims 10, 16, and 18 have been finally rejected under 35 U.S.C. §103(a) as being unpatentable over Ochiai in view of Kameyama et al. and further in view of Iwamatsu. These rejections are respectfully traversed.

Ochiai discloses an integrated circuit device with an SOI structure and comprising a plurality of transistors, each overlying a resistance layer [52] that is flanked by insulating layers [51] and [55].. The Ochiai semiconductor structure is a "sea-of-gate array" and thus includes no trenches to define device islands. The Examiner implicitly acknowledges this lack of trenches with the unsupported assertion that "The insulating region between the transistors can be considered as the trench." (emphasis added).

As was acknowledged in the August 3, 1999 Office Action, Ochiai does not show a resistance layer made of silicide. In fact, Ochiai makes no mention whatsoever of silicides. The deficiencies in the teaching of Ochiai are not remedied by the disclosure in Kameyama of a polycrystalline tungsten silicide resistor thin film formed between two oxide layers and having aluminum electrodes connected at both ends or by the already discussed irrelevant disclosure of Iwamatsu. Withdrawal of the §103(a) final rejections of claims 7-9, 10, 16, and 18 as unpatentable over the combination of these references is therefore respectfully requested.

In the second paragraph on page 7 of the Office Action, the Examiner observes that "fig. 6 shows the buried layer of claim 4 and the diamond layer of claim 5" and then raises the objection that "claims 4 and 5 are depending to claim 1 which discloses the device of figs. 3f and 3g. Neither fig.3f nor fig. 3g discloses the buried layer and the diamond layer."

The patent laws, rules, and MPEP provide no basis for such an objection or rejection. No authority is cited (nor can any be cited) for the position that a claim is unpatentable because no one figure shows all the features of the claim. It is sufficient that the specification disclose the claimed invention.

Because the above amendment of the claims, submitted in accordance with 37 CFR §1.116(a), present them in better form for allowance or consideration on appeal, its admittance is respectfully requested.

Claims 1-5, 7-11, and 13-22 remain in this case. In light of the foregoing Amendment and Remarks, prompt allowance of this application is earnestly solicited.

Respectfully submitted,

Mar. 6, 2000
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